The Abdus Salam International Centre for Theoretical Physics

Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

Organizer(s): Directors: N. Abdallah, A. Cicuttin, A. Marchioro. Local Organizer: M.L. Crespo
Trieste - Italy, 26 October 2009 - 20 November 2009

Final programme

Monday, 26 October 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

08:30 - 11:30	(Room: Adriatico Guest House - Kastler Lecture Hall Area (Lower Level 1)) --- Registration & Administrative Formalities ---
11:30 - 11:45	**C.Tuniz** / *Assistant Director, ICTP* **Opening Address**
11:45 - 12:00	**N. Abdallah** / *Actel Corp., CA, USA* **Course Introduction**
12:00 - 12:15	**A. Cicuttin** / *ICTP* **Course Overview**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	**N. Abdallah** **Introduction to FPGA Synthesis. Introduction to VHDL**
15:30 - 16:00	--- Coffee Break ---
16:00 - 17:00	**N. Abdallah** **Introduction to Actel Prodcuts. Libero IDE Overview and Design Flow**
17:00 - 18:00	**P. Bazargan-Sabet** / *University Pierre & Marie Curie, LIP6, Paris, France* **Introduction to Digital Design**

Tuesday, 27 October 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**P. Bazargan-Sabet** **Digital Design I (Combinatorial elements)**
10:30 - 11:00	--- Coffee Break ---
11:00 - 12:00	**P. Bazargan-Sabet** **Digital Design II (Sequential elements, Mealy and Moore FSM)**
12:00 - 13:00	**N. Abdallah** **Sinthesis I - Introduction to VHDL**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	**N. Abdallah** **Sinthesis II - Introduction to VHDL**
15:30 - 16:00	--- Coffee Break ---
16:00 - 17:00	**N. Abdallah** **(LiberoTM IDE) Design Entry**
17:00 - 18:00	**N. Abdallah** **(LiberoTM IDE) Functional Simulation. Synthesis**

Wednesday, 28 October 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**P. Bazargan-Sabet** **Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc)**
10:30 - 11:00	--- Coffee Break ---
11:00 - 12:00	**P. Bazargan-Sabet** **Digital arithmetic I (number representations)**
12:00 - 13:00	**N. Abdallah** **Synthesis III - Advanced VHDL**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	**N. Abdallah** **(LiberoTM IDE) Place & Route**
15:30 - 16:00	--- Coffee Break ---
16:00 - 17:00	**N. Abdallah** **Design Verification and Timing Concepts**
17:00 - 18:00	**N. Abdallah** **(LiberoTM IDE) Timing Constraints and Analysis**
18:00 - 19:30	--- Reception ---

Thursday, 29 October 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**P. Bazargan-Sabet** **Digital arithmetic II (basic arithmetic operations)**
10:30 - 11:00	--- Coffee Break ---
11:00 - 12:00	**N. Abdallah** **Programmable logic & FPGA architectures**
12:00 - 13:00	**N. Abdallah** **(LiberoTM IDE) Post-Layout Simulation. Programming**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. VHDL Simulation Environment. A design example**
15:30 - 16:00	--- Coffee Break ---
16:00 - 18:00	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits.**

Friday, 30 October 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**N. Abdallah** **Actel Fusion FPGA Architecture**
10:30 - 11:00	--- Coffee Break ---
11:00 - 12:00	**N. Abdallah** **Actel Fusion FPGA Architecture (cont.)**
12:00 - 13:00	(Room: Adriatico Guest House Informatics Lab.) **M. L. Crespo** **Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits.**
15:30 - 16:00	--- Coffee Break ---
16:00 - 18:00	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits (Cont.)**

Monday, 2 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**N. Abdallah** **The Actel Fusion Embedded Development Kit**
10:30 - 11:00	--- Coffee Break ---
11:00 - 12:00	**N. Abdallah** **The Actel Fusion Embedded Development Kit (cont.)**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. Laboratory Session. Finite State Machine: VHDL Description and Simulation (cont.)**
15:30 - 16:00	--- Coffee Break ---
16:00 - 18:00	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. Laboratory Session. Finite State Machine: VHDL Description and Simulation (cont.)**

Tuesday, 3 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. Synthesis and Post-Synthesis Simulation**
10:30 - 11:00	--- Coffee Break ---
11:00 - 13:00	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. Synthesis and Post-Synthesis Simulation (cont.)**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. Synthesis and Post-Synthesis Simulation (cont.)**
15:30 - 16:00	--- Coffee Break ---
16:00 - 18:00	(Room: Adriatico Guest House Informatics Lab.) **M.L. Crespo** **Laboratory Session. Synthesis and Post-Synthesis Simulation (cont.)**

Wednesday, 4 November - Presentations by Participants (Room:Adriatico Guest House Kastler Lecture Hall)

4 November 2009

09:30 - 10:30	**Presentation of FPGA Projects by Participants and Discussion** FPGA Video Processing Platform (A.M. Ariabella - National Univeristy of San Luis, Argentina) 20'

General Projects in LACTEC Research Lab (A.A. Barbiero - LACTEC, Curibita, Brazile) 20'

FPGA Implementation of Neural Networks (A.K. Radi - Ain Shams University, Cairo, Egypt) 20'

10:30 - 11:00 --- Coffee Break ---

11:00 - 13:00 **Presentation of FPGA Projects by Participants and Discussion (cont.)**

Middleware Switch Testing (M. Faisal - University of Rostock, Bremen, Germany) 20'

Residue-to-Decimal Converters for Moduli Sets with Common Factors (K.A. Gbolagade - University of Development Studies, Navrongo, Ghana) 20'

Minimization of Reversible Logic Circuits (Md. S. Islam - University of Dhaka, Dhaka, Bangladesh) 20'

Design of a Distributed Shared Memory for Switch Fabric on FPGA (H. Khani - Islamic Azad University, Semnan, Islamic Republic of Iran) 20'

FPGA-Based Correlation for Random Signal Processing in Noise Radar (O. Melnykova and S. Lukin - Usikov Institute of Radiophysics & Electronics, Kharkiv, Ukraine) 20'

Solar Tracking System using FPGA (L.A. Moreno Coria - Benemerita Universidad Autonoma de Puebla, Puebla, Mexico) 20'

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 **Presentation of FPGA Projects by Participants and Discussion**

Hardware Architechture for Particle Swarm Optimization Algorithm using Floating-Point Arithmetic (D.M. MUNOZ ARBOLEDA - University of Brasilia, Brasillia D.F., Brazil) 20'

FPGA Leap from Microcontrollers (A.K. Bett - University of Nairobi, Nairobi, Kenya) 20'

Lock-In Amplifier (Y. Rumyantsev - Lomonosov Moscow State University, Moscow, Russian Federation) 20'

15:30 - 16:00 --- Coffee Break ---

16:00 - 18:00 **Presentation of FPGA Projects by Participants and Discussion**

Realization of Reconfigurable on Board Architecture Computer for Satellites using FPGA (A. Sadiq - Nigerian Communicatins Satellite Ltd., Abuja, Nigeria) 20'

Microcontrollers in Electronic Security Systems (C. Tchapga Tchito - University of Dschang, Dschang, Repubic of Cameroon) 20'

General Discussion 01h20'

Thursday, 5 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30 **A. Cicuttin**
Selected Topics on Logic Synthesis and FPGA Debugging

10:30 - 11:00 --- Coffee Break ---

11:00 - 12:00 **A. Cicuttin**
Selected Topics on Logic Synthesis and FPGA Debugging (cont.)

12:00 - 13:00 (Room: Adriatico Guest House Informatics Lab.)
C. Sosa Paez / *UNSL, San Luis, Argentina*
Laboratory Session. Hardware Description of the FPGA Development Platform.

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 (Room: Adriatico Guest House Informatics Lab.)
C. Sosa Paez
Laboratory Session. Hardware Description of the FPGA Development Platform (cont.)

15:30 - 16:00 --- Coffee Break ---

16:00 - 18:00 (Room: Adriatico Guest House Informatics Lab.)
C. Sisterna / *UNSJ, San Juan, Argentina*
Laboratory Session. FPGA Implementation Example.

Friday, 6 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30 **A. Cicuttin**
Reconfigurable Virtual Instrumentation (RVI) based on FPGA

10:30 - 11:00 --- Coffee Break ---

11:00 - 12:00 **A. Cicuttin**
Reconfigurable Virtual Instrumentation (RVI) based on FPGA (cont.)

12:00 - 13:00 (Room: Adriatico Guest House Informatics Lab.)
N. Abdallah
System-on-Chip Concepts.

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 (Room: Adriatico Guest House Informatics Lab.)
N. Abdallah
System-on-Chip Concepts (cont.)

15:30 - 16:00 --- Coffee Break ---

16:00 - 18:00 (Room: Adriatico Guest House Informatics Lab.)
M.L. Crespo
Laboratory Session. Implementation in the FPGA Development Platform

Monday, 9 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30 **M. Nolich** / *University of Trieste, Italy*
Introduction to Digital Signal Processing

10:30 - 11:00 --- Coffee Break ---

11:00 - 13:00 **M. Nolich**
Discrete Time Signals and Systems

13:00 - 14:30 --- Lunch Break ---

14:30 - 15:30 (Room: Adriatico Guest House Informatics Lab.)
M.A. Risco Castillo / *Technological University of Peru, Lima, Peru*
The µLab Virtual Pannel

15:30 - 16:00 --- Coffee Break ---

16:00 - 18:00	(Room: Adriatico Guest House Informatics Lab.) **M. Risco Castillo** **The µLab Virtual Pannel. A design example.**

Tuesday, 10 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**A. Kluge** / *CERN, Geneva, Switzerland* **Advanced FPGA Applications**
10:30 - 11:00	--- Coffee Break ---
11:00 - 13:00	**A. Kluge** **A case study in HEP experiments (I)**
13:00 - 14:00	--- Lunch break ---
14:30 - 15:30	**M. Nolich** **The Z-Transform**
15:30 - 16:00	--- Coffee Break ---
16:00 - 17:00	**M. Nolich** **Sampling of Continuous-Time Signals**
17:00 - 18:00	(Room: Adriatico Guest House Informatics Lab.) **M. L. Crespo** **Laboratory Session. Digital Arithmetic.**

Wednesday, 11 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30	**A. Kluge** **A case study in HEP experiments (II)**
10:30 - 11:00	--- Coffee Break ---
11:00 - 12:00	**A. Kluge** **A case study in HEP experiments (III)**
12:00 - 13:00	**M. Nolich** **The Discrete Fourier Transform**
13:00 - 14:30	--- Lunch break ---
14:30 - 15:30	**M. Nolich** **Transform Analysis of LTI Systems**
15:30 - 16:00	--- Coffee Break ---
16:00 - 17:00	**M. Nolich** **Digital Filters Design**

17:00 - 18:00 (Room: Adriatico Guest House Informatics Lab.)
M. L. Crespo
Laboratory Session. Digital Arithmetic (cont.)

Thursday, 12 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30 **K.M. Khare** / *RRCAT, Indore, India*
FPGA-based Custom Board Design for Instrumentation

10:30 - 11:00 --- Coffee Break ---

11:00 - 13:00 **C. Sisterna**
Advanced VHDL Subjects

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 (Room: Adriatico Guest House Informatics Lab.)
M.L. Crespo
Laboratory Session: Waveform generation

15:30 - 16:00 --- Coffee Break ---

16:00 - 18:00 (Room: Adriatico Guest House Informatics Lab.)
M.L. Crespo
Laboratory Session: Waveform generation (cont.)

Friday, 13 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30 **C. Sisterna**
Advanced FPGA Subjects

10:30 - 11:00 --- Coffee Break ---

11:00 - 12:00 **C. Sisterna**
Advanced FPGA Subjects (cont.)

12:00 - 13:00 **M. Nolich**
Digital Filters Design (cont.)

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 (Room: Adriatico Guest House Informatics Lab.)
K.M. Khare
Laboratory Session: ICTP RVI Platform Description

15:30 - 16:00 --- Coffee Break ---

16:00 - 17:00 (Room: Adriatico Guest House Informatics Lab.)
M. Risco Castillo, J. Lopez Botero
Laboratory Session: DEMO: ICTP RVI Platform. Virtual Instruments: Waveform Generator and Digital Oscilloscope (cont.)

17:00 - 18:00 (Room: Adriatico Guest House Informatics Lab.)
K.M. Khare
Laboratory Session: ICTP RVI Platform. A Design Example.

Monday, 16 November 2009 (Room:Adriatico Guest House Kastler Lecture Hall)

09:30 - 10:30 **F. Mammano** / *University of Padova, Italy*
Introduction to two-dimensional digital signal processing

10:30 - 11:00 --- Coffee Break ---

11:00 - 13:00 **F. Mammano**
Two-dimensional digital signal processing

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 **F. Mammano**
Three-dimensional deconvolution in FPGA

15:30 - 16:00 --- Coffee Break ---

16:00 - 18:00 (Room: Adriatico Guest House Informatics Lab.)
C. Sosa Paez
Laboratory Session: Digital Signal Processing with FPGA. A design example.

Tuesday, 17 November 2009 (Room:Adriatico Guest House Informatics Lab.)

09:30 - 10:30 **Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.**

10:30 - 11:00 --- Coffee Break ---

11:00 - 13:00 **Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**

13:00 - 14:30 --- Lunch break ---

14:30 - 15:30 **Visit to and Presentation of the ICTP Multidisciplinary Laboratory (ICTP-MLAB)**
ICTP MLAB ? Multidisciplinary Laboratory (M.L. Crespo) 20'
Applications and Preliminary Results of XDXL (Dipak Debnath, Debashis Bhowmick, Nicola Zampa) 20'
Neurotelemetry ? An RVI Application of Digital-Radio Transmission of Neuronal Signals (M. Risco Castillo) 20'

15:30 - 16:00 --- Coffee Break at the MLAB ---

16:00 - 18:00 **Visit to and Presentation of the ICTP Multidisciplinary Laboratory (ICTP-MLAB)**
Development of a Portable X-Ray Instrumentation for Non Destructive Characterization of Archaeological and Artistic Materials (Federico Bernardini) 20'
Using Neutron Activation Analysis to Characterize Archaeological Samples (Joseph Bremang Tandoh) 20'
Stable Isotope Technique in the Evaluation of Soil Physical Quality (Mutiu A. Busari) 20'
Description of the Experimental DPF set-up at ICTP (A. Cicuttin) 20'

Wednesday, 18 November 2009 (Room:Adriatico Guest House Informatics Lab.)

09:30 - 10:30	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
10:30 - 11:00	--- Coffee Break ---
11:00 - 13:00	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
13:00 - 14:00	--- Lunch break ---
14:30 - 15:00	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
15:30 - 16:00	--- Coffee Break ---
16:00 - 18:00	(Room: Leonardo da Vinci Building Main Lecture Hall) **Darwin & Modern Science** More details on: http://pio.ictp.it/words/news/2009/darwin-and-modern-science

Thursday, 19 November 2009 (Room:Adriatico Guest House Informatics Lab.)

09:30 - 10:30	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
10:30 - 11:00	--- Coffee Break ---
11:00 - 13:00	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
13:00 - 14:00	--- Lunch break ---
14:30 - 15:30	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
15:30 - 16:00	--- Coffee Break ---
16:00 - 18:00	(Room: Adriatico Guest House Kastler Lecture Hall) **Distribution of Diplomas of Attendance**
18:30 - 20:00	(Room: Adriatico Guest House Cafeteria) --- Get-Together ---

Friday, 20 November 2009 (Room:Adriatico Guest House Informatics Lab.)

09:30 - 10:30	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
10:30 - 11:00	--- Coffee Break ---
11:00 - 13:00	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
13:00 - 14:00	--- Lunch break ---
14:30 - 15:30	**Laboratory Session. RVI Projects. Digital Signal Processing with FPGA**
15:30 - 16:00	--- Coffee Break ---

16:00 - 18:00 Laboratory Session. RVI Projects. Digital Signal Processing with FPGA